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Hard mask processing of 20% efficiency back-contacted silicon solar cells with dopant-free heterojunctions

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ABSTRACT

Single junction crystalline silicon (c-Si) solar cells featuring a conventionally doped interdigitated back contact heterojunction (IBC-SHJ) structure has approached a record efficiency of 26.6%, which is very close to the practical limit. However, integrating the interdigital *p*- and *n*-type amorphous silicon (a-Si:H) layers on the rear surface of Si substrate is of such complexity, posing problem of heavy dependences on expensive manufacturing techniques including plasma-enhanced chemical vapor deposition and photolithography. Its commercial potential is thus always being questioned, and to seek an alternative fabrication procedure, which adapts to cost-effective deposition parallel with simple patterning characteristics, has been a primary research target of related subjects. Here, we demonstrated 20.1% efficiency dopant-free IBC-SHJ solar cells by combining evaporated carrier-selective materials (MoO_x and LiF_x) and two-steps hard masks alignments, delivering substantial simplifications in the architecture and fabrication procedures. We investigated the effect of intrinsic a-Si:H films with different thicknesses on the passivation and contact resistance for both a-Si:H/MoO_x and a-Si:H/LiF_x contacts, showing 4 nm a-Si:H is better for high efficiency IBC-SHJ solar cells. We also found that the position of the metal target (electrode definition step) and isolation in between the busbar and the Si substrate are highly relevant to leakage and recombination and have great impact on the device performance. The dopant-free IBC-SHJ solar cells demonstrated here manifest enough confidence in our hard mask based fabrication procedure, with great potential for high performance-to-cost ratio in future.

1. Introduction

Interdigitated back contact silicon heterojunction (IBC-SHJ) solar cells combine the advantages of both IBC and SHJ structures, posing a great potential for extremely high power conversion efficiency (*PCE*) [1]. At present, crystalline silicon (c-Si) solar cells with IBC-SHJ structure have achieved a record *PCE* of 26.6%, which is very close to the practical *PCE* limit (around 29%) for single-junction solar cells [2]. The IBC structure can achieve high short-circuit current density (J_{sc}) by eliminating metal grid shading at the front surface, and the SHJ structure can provide high open-circuit voltage (V_{oc}) due to the excellent passivation from intrinsic hydrogenated amorphous silicon (a-Si:H) on the c-Si surface. This class of doped IBC-SHJ solar cells is the focus of breakthrough on efficiency in the current and future. However, excessively complex manufacturing processes and intolerant to high temperature annealing procedure (required by metallization) raise concerns about their high-volume production. The complex processes of doped IBC-SHJ solar cells are mainly derived from the formation of interdigitated *p*- and *n*-type a-Si:H strips, which are usually implemented by multiple photolithographic patterning, as well as several wet-chemical etching and cleaning processes. In addition, the photoelectric losses inherent to the doped layers themselves restrain further promotion on efficiency. Thus, cost-competitiveness of IBC-SHJ largely relies on development of low-complexity processing and industry-relevant fabrication methods as well as new functional materials corresponding to them.

Recently, the emerging carrier-selective materials seem to be ideal candidates for easily constructing IBC-SHJ solar cells, because they can always be processed by low-temperature evaporation or even spinning-coating. By well selection of the functional materials as well as smart designs of the band alignments, effective carrier-selective contacts aiming to extract only one-type of carrier (holes or electrons) while

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blocking the other are achievable without using the doped *p*- or *n*-type a-Si:H. So far, many alternative materials have been developed successfully, including organic polymers [3–6] and transition metal oxides (TMOs) [7–11], [e.g., molybdenum oxide (MoO_x), vanadium oxide (VO_x) and tungsten oxide (WO_x)], as hole-selective contacts and metal oxides [12–15] [e.g., magnesium oxide (MgO_x), titanium oxide (TiO_x)], alkaline salts [16,17] [e.g., magnesium fluoride (MgF_x), lithium fluoride (LiF_x)], *etc*, as electron-selective contacts. Complex fabrication route in conventional IBC-SHJ is thus eliminated by applying the abovementioned new functional materials. In recent years, dopant-free IBC-SHJ solar cells with *PCE* beyond 15% have been reported [8,18]. However, due to the poor passivation of the rear side, the efficiency of the solar cells was limited. The *PCE* of dopant-free IBC-SHJ solar cells were then significantly improved by adding a passivation layer in the gap region [19,20]. Besides, in a conference paper [21], Shen et al. reported an efficiency up to 22.2% of dopant-free IBC-SHJ solar cells by using a-Si:H as back surface passivation layer and MgF_x as additional antireflection layer.

Here, we fabricated IBC solar cells with dopant-free heterocontacts using a-Si:H as rear surface interfacial passivation layer, and MoO_x and LiF_x as the back-sided hole- and electron-selective layers, respectively. More important, in the fabrication of IBC-SHJ devices, we use a simple method to form interdigitated *p*- and *n*-type strips and corresponding metal layers by hard masks, requiring only two masking steps instead of the multi-steps photolithographic patterning. Firstly, the passivation behavior of the interfacial thin a-Si:H layer and the effect of its thickness on the carrier transport were explored. The optical and electrical properties of the thermally evaporated MoO_x/Ag hole-selective contact and LiF_x/Al electron-selective contact on *n*-Si, were then thoroughly investigated. Finally, in order to reduce edge leakage, we adjusted the position of the metal target to obtain electrode strips with sharp edges. By combining above essentials together, we fabricated dopant-free IBC-SHJ solar cells with *PCE* above 20%, which shows enormous potential for boosting performance-to-cost ratio in future.

2. Results and discussion

To evaluate the passivation performance of the c-Si/a-Si:H interface, the thickness-dependent effective minority carrier lifetime as well as effective surface recombination velocities (S_{eff}) on a-Si:H film are characterized and shown in Fig. 1(a). As the a-Si:H film thickness increases from 0 to 8 nm, the effective minority carrier lifetime increases significantly. With further increasing the a-Si:H film thickness, the effective minority carrier lifetime keeps near a constant. When the thickness of a-Si:H film is greater than 8 nm, the minority carrier lifetime exceeds 1.8 ms and the S_{eff} is less than 5 cm/s, which exhibits excellent surface passivation. Note that the relatively low S_{eff} value of the bare silicon is the effect of hydrogen passivation, since the silicon wafer was dipped in hydrofluoric (HF) acid solution before testing. The implied V_{oc} at one sun can be extracted from the injection-dependent carrier lifetime τ (Δn), as illustrated in Fig. 1(b). The LiF_x/Al stack provides poor passivation to c-Si surface, corresponding to an implied V_{oc} of only 516 mV. In order to improve the passivation quality of the c-Si interface, excellent passivation materials are required. While a-Si:H has been shown to provide high quality passivation of c-Si surfaces [22–24]. An implied V_{oc} value of 711 mV was achieved on our sample with 4 nm a-Si:H layer. When inserting 4 nm a-Si:H layer between LiF_x and *n*-Si, the implied V_{oc} increases markedly from 516 mV to 697 mV. In comparison with the a-Si:H passivated wafer, the implied V_{oc} decreases after depositing LiF_x film, probably due to a certain degree of thermal damage to the a-Si:H layer when depositing LiF_x film. The implied V_{oc} of MoO_x without (633 mV) and with (696 mV) 4 nm a-Si:H film are shown in Fig. S1.

In order to evaluate the electrical behavior of the different rear contacts, the contact resistivity (ρ_c) was measured using the method designed by Cox and Strack [25,26]. Fig. S2 shows the extraction processes of ρ_c for different samples. The typical *I-V* curves for the different samples of *n*-Si/0.5 nm LiF_x/Al, *n*-Si/4 nm a-Si:H/0.5 nm LiF_x/Al, *n*-Si/10 nm MoO_x/Ag, *n*-Si/4 nm a-Si:H/10 nm MoO_x/Ag, which were collected from the same electrode diameter (2 mm), are shown in Fig. 1(c). The *n*-Si/LiF_x/Al and *n*-Si/a-Si:H/LiF_x/Al contacts show linear *I-V* curve, achieving an Ohmic contact. This directly verified the effectiveness of the LiF_x layer for electron-selective transport. And the current of *n*-Si/a-Si:H/LiF_x/Al is slightly lower than that of *n*-Si/LiF_x/Al, mainly due to the additional resistive barrier associated with the bulk resistance of a-Si:H. Meanwhile, the *n*-Si/MoO_x/Ag and *n*-Si/a-Si:H/MoO_x/Ag contacts show the measured *I-V* curves with typical Schottky rectifying characteristics. This rectification effect stems from the work function difference between the MoO_x and *n*-Si, and the right shifted *I-V* curve for *n*-Si/a-Si:H/MoO_x/Ag sample is due to the additional interfacial resistance as well as the bulk resistance of a-Si:H itself. Fig. 1(d) shows that the ρ_c value of the *n*-Si/a-Si:H/0.5 nm LiF_x/Al and *n*-Si/a-Si:H/10 nm MoO_x/Ag stacks have a strong dependence on the a-Si:H layer thickness. The *n*-Si/a-Si:H/LiF_x/Al stack has a low ρ_c due to excellent Ohmic contact to *n*-Si. With the a-Si:H thickness increases from 0 to 8 nm, the ρ_c increases from 4 to 83 $m\Omega\,cm^2$. However, the *n*-Si/a-Si:H/MoO_x/Ag stack has a relatively high ρ_c. This is due to the presence of the barrier resulting from the valence band offset between c-Si and a-Si:H, which hinders the extraction of holes [7]. With the thickness of a-Si:H increases, the ρ_c of *n*-Si/a-Si:H/MoO_x/Ag stack increase significantly. Therefore, although the contact passivation is greatly improved by increasing the thickness of the a-Si:H interlayer, too thick a-Si:H layers will cause unacceptable increase in ρ_c due to the low conductivity of a-Si:H layer.

To further evaluate the passivation and contact performances of the IBC-SHJ solar cells, Fig. 2(a) shows the simulated efficiency for IBC-SHJ solar cell as a function of the rear contact S_{eff}, $\rho_{c\text{-}HTL}$ and $\rho_{c\text{-}ETL}$. It can be observed that the *PCE* is positively correlated to the improved passivation quality and reduced $\rho_{c\text{-}HTL}$ and $\rho_{c\text{-}ETL}$. The red data points correspond to the potential efficiency of our IBC-SHJ solar cells with different a-Si:H thicknesses. As the thickness of a-Si:H interlayer increases, the S_{eff} of the rear contact decreases gradually, but $\rho_{c\text{-}HTL}$ and $\rho_{c\text{-}ETL}$ increase significantly. Therefore, the thickness of a-Si:H interlayer should be chosen properly. We found that the IBC-SHJ solar cells with 2 nm-thick or 4 nm-thick a-Si:H interlayer have a simulated efficiency close to 24% due to the low S_{eff} as well as the tolerable $\rho_{c\text{-}HTL}$ and $\rho_{c\text{-}ETL}$ of the rear contacts. Fig. S3 shows the corresponding simulated V_{oc} (a), J_{sc} (b) and fill factor (*FF*) (c) of Fig. 2(a) as a function of the rear contact S_{eff}, $\rho_{c\text{-}HTL}$ and $\rho_{c\text{-}ETL}$. We can observe that the V_{oc} and J_{sc} are mainly determined by S_{eff}, and they are significantly improved as reducing the S_{eff}. While the *FF* is determined by the S_{eff}, $\rho_{c\text{-}HTL}$ and $\rho_{c\text{-}ETL}$. To improve *FF*, it is necessary to simultaneously reduce the rear contact S_{eff}, $\rho_{c\text{-}HTL}$ and $\rho_{c\text{-}ETL}$.

We utilize the free energy loss analysis (FELA) output data to present a detailed loss analysis of the investigated cells at the maximum power point (MPP). Fig. 2(b) shows the electrical power loss of different IBC-SHJ solar cells (without and with 4 nm a-Si:H interlayer) at MPP. The bars are subdivided into different loss mechanisms. The major loss contributors of the IBC-SHJ solar cell without a-Si:H layer are the electron-transporting layer (ETL) and gap region recombination losses as well as resistive loss of hole in bulk *n*-Si. The recombination losses mainly caused by the electrical shading effect. Since the hole-transporting layer (HTL) interdigitated with ETL on the rear side, the photogenerated minority carriers (holes in *n*-Si) above HTL have a large probability of being transported to HTL, while holes above the non-collecting region (including ETL and gap region) have a large probability of being recombined if the noncollecting region has poor passivation [27,28]. The resistive loss of holes was caused by the low concentration of holes in bulk *n*-Si. Under illumination conditions, the hole conductivity formula is $\sigma_p = q(p_0 + \Delta p)\mu_p$, (where q is the charge of electron, p_0 is the concentration of holes in the Si wafer at the condition of thermal equilibrium, Δp is the excess carrier concentration, μ_p

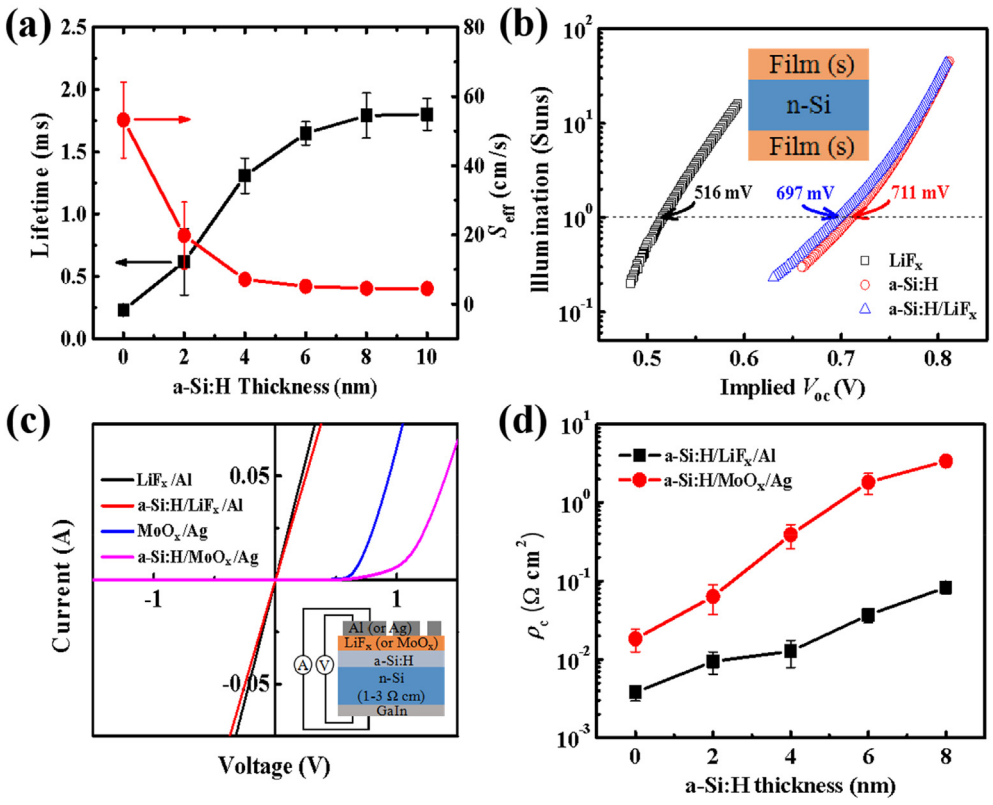

Fig. 1. (a) Effective minority carrier lifetime and surface recombination velocities versus a-Si:H film thickness. (b) The implied V_{oc} behavior for *n*-Si wafers symmetrically coated with a-Si:H, LiF_x or a-Si:H/LiF_x, respectively. The dotted horizontal line highlights the implied V_{oc} at 1 sun. Inset shows the schematic structure for the carrier lifetime and implied V_{oc} tests. (c) Typical *I-V* curves (collected from a pad with diameter of 2 mm) for Si/LiF_x/Al and Si/MoO_x/Ag contacts without or with a-Si:H. Inset shows the schematic structure for the contact resistivity test. (d) The ρ_c of Si/a-Si:H/LiF_x/Al and Si/a-Si:H/MoO_x/Ag as a function of a-Si:H interlayer thickness. These error bars are based on the measured spread in data or the estimated error in the measurement (whichever is largest).

is the hole mobility). In *n*-Si wafer, p_0 is much smaller than Δp. Thus, the σ_p is mainly determined by the Δp. In order to visually observe the Δp in the cells, we simulated the value of Δp by software, as shown in Fig. S4. We can see that the IBC-SHJ solar cell without a-Si:H interlayer has a relatively low Δp. Therefore, the σ_p is low, resulting in a high resistive loss of hole in bulk *n*-Si.

From the results, we can clearly see that the recombination losses (including ETL and gap region recombination losses) and resistive loss (hole in bulk *n*-Si) of the IBC-SHJ solar cell with 4 nm a-Si:H layer are significantly reduced, due to improved passivation to the *n*-Si wafer. The major loss contributors of the 4 nm a-Si:H layer involved sample are the HTL resistive loss and bulk recombination loss. When the 4 nm a-Si:H layer was inserted, although the passivation quality was remarkably improved, the contact resistance of the HTL layer was significantly increased. We need to optimize the HTL contact characteristics to reduce the resistance loss. The bulk recombination loss is related to an increase in the excess carrier concentration of the Si wafer. Since the occurrence of recombination depends on the hole concentration (p), the electron concentration (n) and the recombination probability at that point, which is proportional to np. And $n = n_0 + \Delta n$, $p = p_0 + \Delta p$, (n_0 is the electron concentration in the Si wafer at the condition of thermal equilibrium), which means that the recombination has a direct positive correlation with the excess carrier concentration. It can be seen from Fig. S4, when inserting 4 nm a-Si:H layer, the excess carrier concentration increases, which leads to an enhanced chance for electron-hole recombination. This indicates that the main recombination loss comes from the bulk recombination loss of the Si wafer, when the surface of the Si wafer has excellent passivation. It should be noted that the bulk lifetime of our Si wafers is approximately 5 ms, so the bulk recombination is relatively high. In order to further reduce the bulk recombination loss, it is necessary to utilize Si wafers with ultra-higher carrier lifetime. Fig. S5 shows the simulated efficiency of IBC solar cells as a function of the bulk lifetime. As the bulk lifetime of the Si wafer increased from 0.1 ms to 100 ms, the simulated efficiency of IBC-SHJ solar cells increased from 15.3% to 27.1%.

During the device fabrication processes, we found that the exposure

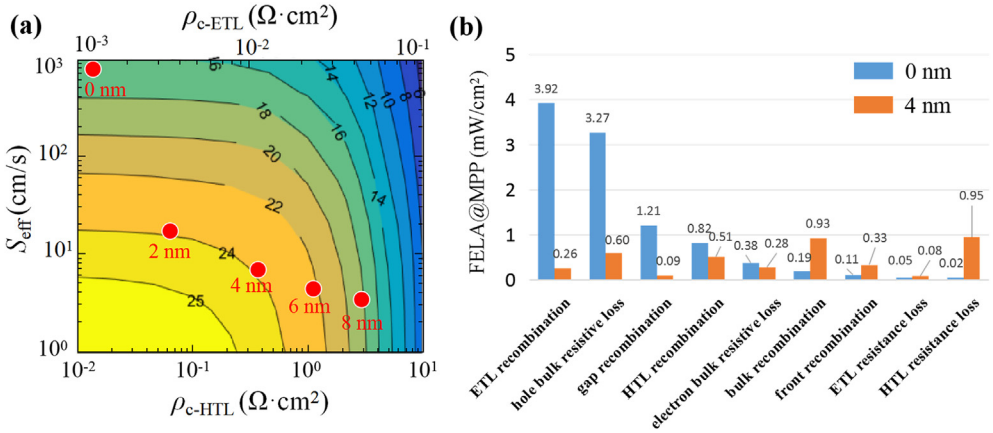

Fig. 2. (a) Simulated ideal efficiency (colored contours) for IBC-SHJ solar cells as a function of the rear contact S_{eff}, $\rho_{c\text{-}HTL}$ and $\rho_{c\text{-}ETL}$. The red data points represent the potential efficiency of our IBC-SHJ solar cells with different a-Si:H thickness. The S_{eff}, $\rho_{c\text{-}HTL}$ and $\rho_{c\text{-}ETL}$ were derived from Fig. 1. Here, $S_{HTL} = S_{ETL} = S_{gap} = S_{eff}$, and the range of $\rho_{c\text{-}HTL}$ as well as $\rho_{c\text{-}ETL}$ are 0.01–10 Ω cm^2 and 0.001–0.1 Ω cm^2, respectively. (b) The free energy loss analysis (FELA) of different IBC-SHJ solar cells (without and with a-Si interlayer) at max power point (MPP).

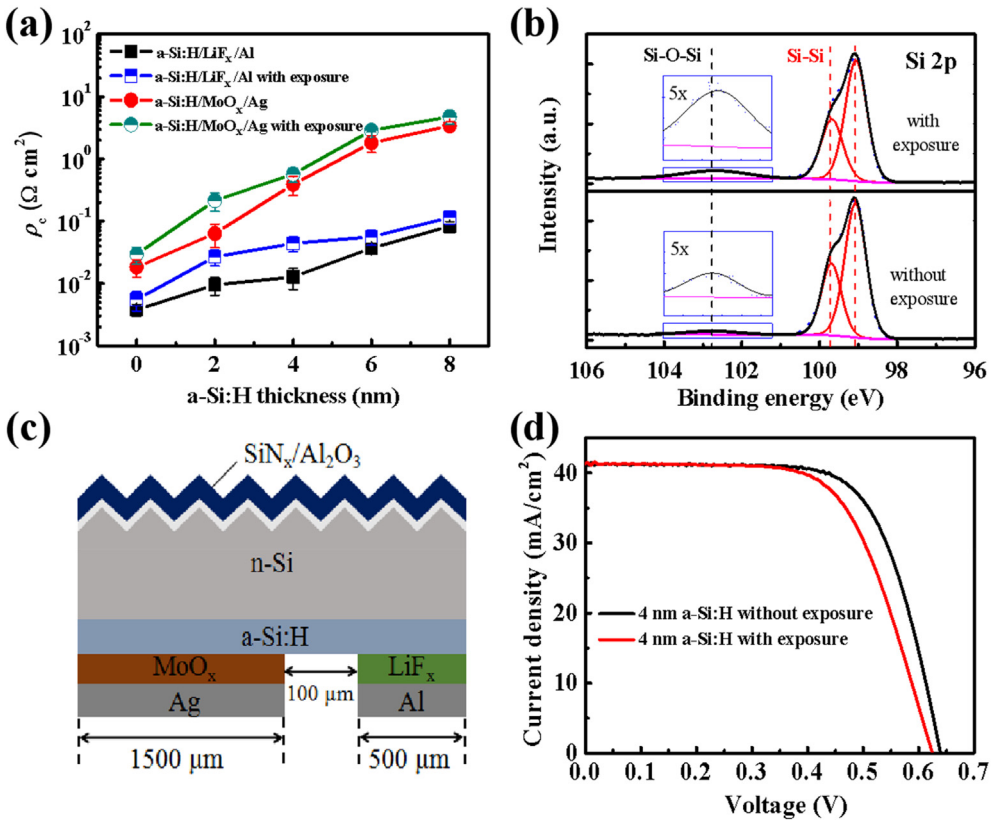

Fig. 3. (a) The ρ_c of Si/a-Si:H/LiF_x/Al and Si/a-Si:H/MoO_x/Ag as a function of a-Si:H interlayer thickness for the a-Si:H with/without 6-h' exposure to air. (b) The XPS spectra for the a-Si:H samples with and without 6-h' exposure to air. (c) The schematic structure of the dopant-free IBC-SHJ solar cell. (d) The light *J-V* curves of the IBC-SHJ solar cells featuring 4 nm a-Si:H layer with/without air exposure.

time for the a-Si:H to air do has a critical effect on the contact resistance. Fig. 3(a) shows the change in ρ_c corresponding to Fig. 1(d) when the a-Si:H layer was exposed to air for 6 h. We found an obvious increase in the ρ_c of Si/a-Si:H/LiF_x/Al and Si/a-Si:H/MoO_x/Ag for all varied thicknesses of a-Si:H layer after 6-h' exposure of a-Si:H to air. To investigate the reason for the measured increase in ρ_c, Fig. 3(b) shows the x-ray photoelectron spectra (XPS) of Si 2p for different samples: *i*) as-deposited a-Si:H; *ii*) a-Si:H after 6-h' exposure to air. The Si 2p spectra can be divided into two bands: one at lower binding energy (99.1 eV and 99.7 eV) attributed to Si-Si bonds and the other at higher binding energy (102.8 eV) attributed to Si-O-Si bonds. We can observe that the intensity of SiO_x peak increase when a-Si:H layer was exposed to air for 6 h. This indicates a thin oxide layer could be grown on the surface of a-Si:H layer after being exposed to air for several hours, which in turn is responsible for the measured increase in ρ_c. The XPS of O 1s for the a-Si:H samples with and without 6-h' exposure to air are shown in Fig. S6.

The schematic structure of IBC-SHJ solar cell is shown in Fig. 3(c), illustrating a HTL region (*n*-Si/a-Si:H/MoO_x/Ag) of 1500 μm, an ETL region (*n*-Si/a-Si:H/LiF_x/Al) of 500 μm, and the region between HTL and ETL ("gap") of 100 μm. The substrate in the method is a single-side textured *n*-Si wafer with a front textured surface and a polished rear surface for the emitters and BSF. At the front side, a stack of Al_2O_3 and SiN_x was deposited to serve as surface passivation and antireflection coating. This surface preparation minimizes optical losses and provides efficient front surface passivation. The rear surface of the *n*-Si wafer is passivated by a-Si:H layer, then the MoO_x/Ag and LiF_x/Al structures were interdigitated on the rear side, serving as hole- and electron-selective contacts, respectively. The detailed processing flow for this kind of dopant-free IBC-SHJ solar cells is shown in Fig. S7.

Fig. 3(d) shows the light *J-V* curves of the IBC-SHJ solar cells featuring 4 nm a-Si:H layer (with/without air exposure). The black line represents the reference solar cell, and the red line is that the a-Si:H was exposed to air for 6 h before depositing the following materials. When a-Si:H layer was exposed to air for 6 h, V_{oc} of the solar cell decreased from 639 mV to 625 mV and *FF* decreased from 68.9% to 64.3%. This shows that the oxidation on the surface of the a-Si:H layer will degrade both the passivation quality as well as the contact property. Therefore, after depositing the a-Si:H layer, the sequential material should be deposited on its surface in time.

The photovoltaic parameters of the IBC-SHJ solar cells featuring a-Si:H films with varied thickness are summarized in Table 1. The devices without a-Si:H layer exhibited a relatively low *PCE* of 12.2%, with V_{oc} of 562 mV, J_{sc} of 35.5 mA/cm^2 and *FF* of 61.3%. The high defect density on the silicon surfaces results in low V_{oc} and J_{sc}. After applying the a-Si:H layer on the rear side of the *n*-Si, the *PCE* was obviously improved. The solar cell with 4 nm a-Si:H film obtained the highest *PCE* of 18.1%, associated with V_{oc}, J_{sc}, and *FF* values of 639 mV, 41.2 mA/cm^2, and 68.9%, respectively. As shown in Table 1, as the thickness of the a-Si:H layer increases, the V_{oc} and J_{sc} increase significantly, but the *FF*

Table 1
The photovoltaic parameters of the IBC-SHJ solar cells with different a-Si:H layer thickness.

Thickness (nm)	V_{oc} (mV)	J_{sc} (mA/cm^2)	*FF* (%)	η (%)	R_s (Ω·cm^2)	R_{sh} (Ω·cm^2)
0 nm	562 (560 ± 6)	35.5 (35.4 ± 0.3)	61.3 (61.0 ± 0.3)	12.2 (12.0 ± 0.4)	1.98 (1.93 ± 0.05)	181 (164 ± 19)
2 nm	614 (611 ± 3)	39.7 (39.5 ± 0.5)	71.9 (71.7 ± 0.6)	17.5 (17.4 ± 0.3)	1.84 (1.87 ± 0.06)	2303 (2208 ± 439)
4 nm	639 (636 ± 5)	41.2 (41.1 ± 0.3)	68.9 (69.1 ± 0.5)	18.1 (18.0 ± 0.5)	2.47 (2.54 ± 0.09)	3939 (3492 ± 578)
8 nm	652 (650 ± 4)	41.6 (41.5 ± 0.4)	63.4 (63.5 ± 0.8)	17.2 (17.1 ± 0.4)	5.20 (5.39 ± 0.17)	1440 (1268 ± 136)

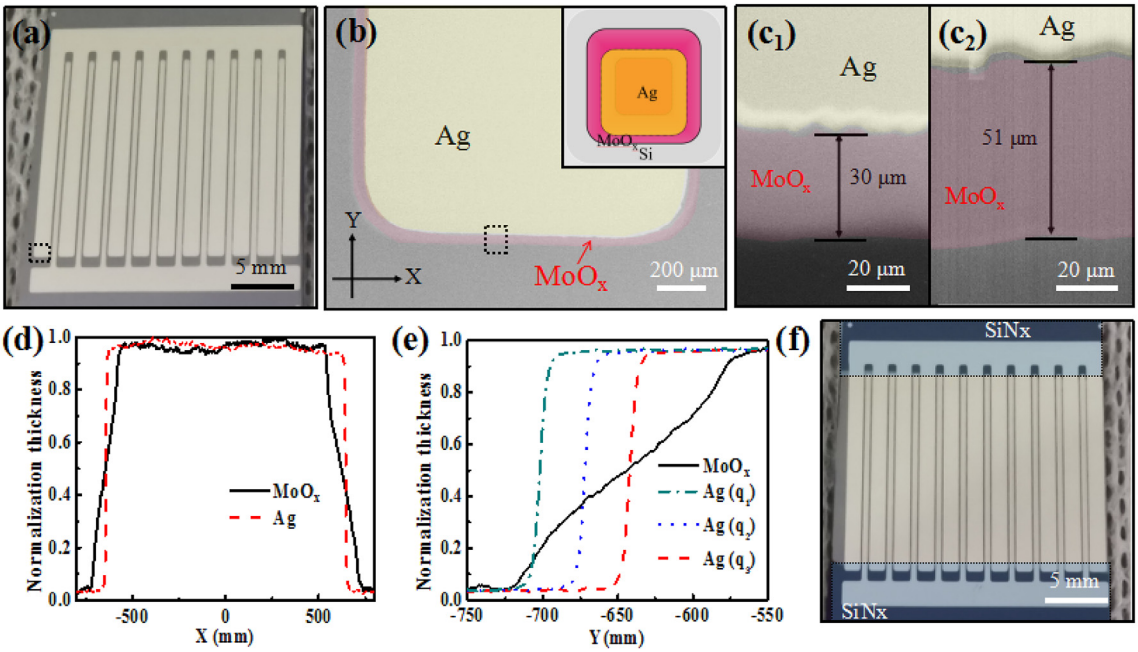

Fig. 4. (a) The optical image of the devices' rear side. (b) Enlarged SEM image of black dashed boxes in Figure (a). (c) Enlarged SEM image (c_1) of black dashed boxes in Figure (b) and corresponding image (c_2) obtained after using the modified evaporation method. (d) The normalization contour lines of MoO_x and Ag films. (e) Simulated shifts of Ag contour lines at different evaporation positions. (f) The optical image of the devices' rear side after adding a SiN_x layer between the busbar and the Si substrate.

decreases drastically. The increase in V_{oc} and J_{sc} is associated with the improved rear surface passivation and reduced interface recombination. The *FF* decreases with increasing a-Si:H layer thickness, which could be caused by the increase in series resistance due to the limitation of charge-carrier transport through the a-Si:H layer. However, the *FF* of the devices without a-Si:H layer is significantly lower than the devices with a-Si:H layer, which may be related to the extremely bad shunt resistance (R_{sh}). Therefore, it should be affirmed that some leakage channels exist.

We prepared the back structure of the device by thermal evaporation. In actual operation, since the position of the evaporation material is not vertical to the substrate, the material was deposited on the substrate at an oblique angle. Fig. S8 shows the principle analysis of the evaporation process. We can find that the larger the oblique angle, the more obvious the Ag electrode deviates from MoO_x. Fig. 4(a) shows the optical image of the devices' rear side. The enlarged SEM image of the black dashed boxes was shown in Fig. 4(b). The inset shows the corresponding schematic diagram of the Ag electrode deviates from MoO_x. In Fig. 4(c_1) and **(c_2)**, we exhibited the enlarged images of black dashed boxes in Fig. 4(b). Where the Ag target was deposited on the substrate with an oblique angle in the left image (c_1) and substantially vertical direction in the right image (c_2). We found that the width of the Ag boundary to the MoO_x boundary increased when the Ag target was deposited vertically on the substrate, indicating a decrease in the offset of the Ag electrode. It should be noted that the MoO_x target was deposited at an oblique angle and simultaneously rotated substrate, while the substrate was not rotated when evaporating Ag. From Fig. 4(d), we can see that the width of the MoO_x film was wider than that of the Ag film. As the Ag boundary gets closer to the MoO_x boundary, the corresponding MoO_x film thickness decreases linearly under the Ag boundary, as shown in Fig. 4(e). In order to reduce the edge leakage, we need to reduce the offset of the silver electrode by depositing silver target vertically on the substrate. Moreover, we added a SiN_x layer between the busbar and Si substrate to eliminate leakage and reduce recombination in this area, as shown in Fig. 4(f).

By adjusting the position of the metal target and isolating the busbar and the Si substrate, our dopant-free solar cell efficiency is significantly improved. The light *J-V* curve together with corresponding electrical parameters of the dopant-free IBC-SHJ solar cell with 4 nm a-Si:H film were presented in Fig. 5(a), showing a *PCE* of 20.1%, associated with a V_{oc}, J_{sc}, and *FF* of 659 mV, 41.6 mA/cm^2, and 73.2%, respectively. Table S1 shows the photovoltaic parameters of the IBC-SHJ solar cells with different fabrication methods. The champion cell batch shows an average efficiency close to 20.0% (see Table S2). The J_{sc} is on a high level, demonstrating the effective light trapping and excellent passivation quality on the front side of the solar cells. The relatively low *FF* may be due to the thin metal electrode (300 nm) of the IBC solar cell, resulting in a relatively large series resistance. Fig. 5(b) presents the corresponding quantum efficiency analysis showing the external quantum efficiency (EQE) and reflectance (R) for the solar cell. The J_{sc} obtained by integrating the EQE curve with an AM 1.5G reference spectrum is 41.5 mA/cm^2, which is agreement with the J_{sc} measured via light *J-V*.

3. Conclusion

In summary, we have fabricated dopant-free IBC-SHJ solar cells with conversion efficiencies above 20% by using only two-steps hard masks alignments, which greatly simplifies the process flows compared to the conventionally doped IBC-SHJ solar cells. We found that the dopant-free IBC-SHJ solar cells with 4 nm a-Si:H layer can achieve high *PCE*. However, low V_{oc} and *FF* values limit our current device efficiency. By further optimizing the passivation quality of the a-Si:H layer, a higher V_{oc} of the device should be achieved. The moderate *FF* values that caused by thin metal electrode may also be improved, in future, by thickening the metal electrodes. Besides, we improved the alignment quality by adjusting the position of the metal target, which reduces edge leakage. Finally, efficiency beyond 24% is highly expected based on our simulation concerning the effects of passivation and contact property on efficiency. This work demonstrated a feasibility of using a simple process flow to fabricate highly efficient and cost-effective dopant-free IBC-SHJ solar cells.

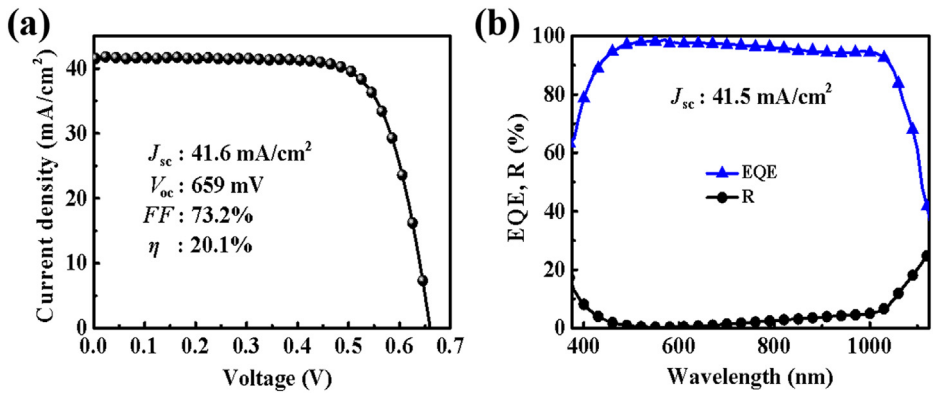

Fig. 5. (a) The light *J-V* characteristic and electrical parameters of the dopant-free IBC-SHJ solar cell with 4 nm a-Si:H interlayer. (b) External quantum efficiency (EQE) and reflectance (R) for the solar cell.

4. Experimental section

Devices Fabrication: Double-sides polished Czochralsk (CZ) *n*-Si wafers with a resistivity of 1–10 Ω cm and a thickness of ~250 μm were used for passivation quality characterization. For the contact resistivity measurements, one-side polished CZ *n*-Si wafers with a resistivity of 1–3 Ω cm and a thickness of ~270 μm were used. The contact resistivity was extracted by the method developed by Cox and Strack. An array of different diameters circular pads was evaporated on the front of the test structures via a shadow mask. A full area GaIn was coated on the rear surface of the contact samples. For IBC-SHJ solar cells fabrication, one-side polished CZ *n*-Si wafers with a resistivity of 1–3 Ω cm and a thickness of ~250 μm were used. The unpolished side of the wafer was textured with a random-pyramids structure by immersing in NaOH and isopropanol solutions with concentration of 2.5% and 1.25%, respectively, at a temperature of 80 °C for 15 min. During the texturing process, the other side of the wafer was protected by a homemade tool. All wafers were cleaned by the standard Radio Corporation of America (RCA) cleaning processes and dipped in a 4% diluted HF solution to remove the native oxide layer. The random-pyramids surface of *n*-Si wafer was passivated by atomic layer deposited (ALD) Al_2O_3 (~15 nm), and then SiN_x film (~75 nm) was deposited as anti-reflection layer by plasma-enhanced chemical vapor deposition (PECVD). Intrinsic hydrogenated amorphous silicon (a-Si:H) films with different thickness (0–8 nm) were deposited on the rear side of the wafers as passivation layer by PECVD. After applying different metal masks, the MoO_x and LiF_x films of 10 nm and 0.5 nm thickness were respectively deposited on the Si rear side by thermal evaporation with a deposition rate of 0.2 Å/s at a base pressure 6.0×10^{-6} Torr. And the corresponding 300 nm thick metal electrodes Ag and Al were separately evaporated onto the surface without breaking the vacuum.

Characterization: The effective carrier lifetime and implied V_{oc} were measured by a Sinton WCT-120 lifetime tester using quasi-steady state photoconductance (QSSPC) methods. The current-voltage (*I-V*) curves of the contact resistivity were measured by a Keithley 4200-scs semiconductor parameter analyzer. The thickness of the a-Si:H films was measured by spectroscopic ellipsometry (Uvisel, Horiba). XPS characterization was performed with a Kratos AXIS Ultra DLD, and all spectra were measured using a monochromatic Al Kα X-ray source and a hemispherical analyzer in ultrahigh vacuum with a base pressure of 1×10^{-10} mbar. The light current density-voltage (*J-V*) curves of solar cells were measured by a Class AAA solar simulator (Oriel, Sol3A) under AM 1.5 illumination (100 mW cm^{-2}) in the standard testing condition. The illumination intensity was calibrated using an encapsulated standard Si solar cell from Newport Corporation. The cells were shielded by an opaque mask with a designated aperture area of 1 cm^2. The EQE curves as well as the reflectance spectra were measured by a quantum efficiency measurement system (QEX10, PV Measurements). The morphological analysis of the samples was conducted by SEM (Hitachi S-4800).

Simulation method: In this simulation, we employ Quokka software to simulate the photoelectric performances of IBC-SHJ solar cells. In device simulation, the main parameters were set as follows: The substrate was *n*-Si wafers with 5 ms bulk lifetime. The thickness of *n*-Si wafers was set as 250 μm, and the resistivity was chosen as 2 Ω cm. The surface recombination velocity of the front Al2O3/Si interface was set as 2 cm/s. The surface recombination velocity of the rear side and the contact resistivity of HTL and ETL were derived from the experimental values of Fig. 1. The dimensions of the devices' ETL, HTL and gap were consistent with the values in Fig. 3.

Acknowledgments

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.nanoen.2019.104116.

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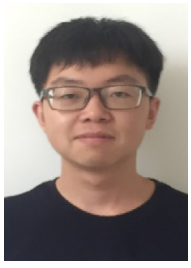

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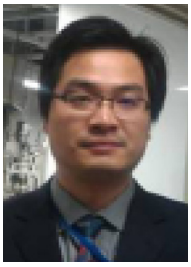

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